The Office Action maintains that the method claims of the present application are inherent to the apparatus claims 2, 6-8, 16, and 64 of 09/902,541. Claim 2 of the copending application recites a digital phase detector circuit for the phase locked loop system. Claim 6 recites a delta-sigma encoder circuit having a clock input coupled to receive a first clock signal. Claim 7 recites a digital accumulator circuit for accumulating successive values of a digital input signal representing the phase error, and for providing on an output thereof a multi-bit accumulated digital phase error signal. Claim 8 recites that the digital accumulator circuit comprises an accumulator circuit for conveying the multi-bit accumulated digital phase error signal having a variable number of bits beginning with the least significant bit. Claim 16 recites a decimator circuit responsive to the digital phase error signal, for generating a decimated digital phase error signal which is coupled to the accumulator circuit as the digital input signal. Claim 64 recites that a digital accumulator circuit comprises a ripple counter circuit.

In contrast, claim 1 of the present application recites a method of acquiring timing associated with an input data stream, comprising detecting whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream; and evaluating whether a phase-locked loop (PLL) has acquired the timing of the input data stream according to occurrence of transitions of the input data stream in the predetermined portion of the sample clock period.

There is nothing described in claims 2, 6-8, 16 and 64 of copending Application No. 09/902,541 that provides detecting whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream. The disclosure of the 09/902,541 application teaches a linear phase detector and the circuitry described in claims 2, 6-8, 16 and 64 describe the phase detector and processing of an error signal indicative of the difference between the input signal and the feedback signal generated by the phase detector. There is nothing inherent or actual in those claims that provide detecting whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream; and evaluating whether a phase-locked loop (PLL) has acquired the timing of the input data stream according to occurrence of transitions of the input data stream in the predetermined portion of the sample clock period as recited in claim 1 of the present application. In fact, co-pending application

09/902,541, teaches use of a reference clock to aid in frequency acquisition (see Fig. 14 and description on page 27). Accordingly, applicant respectfully requests that the rejection of claim 1 and all rejected claims dependent thereon be reconsidered and withdrawn.

Applicants note that claim 16 is in means plus function format. Accordingly, it must be interpreted to cover the corresponding structure, materials or acts in the specification and equivalents thereof. See MPEP 2181. Structure corresponding the claimed means includes, but is not limited to, Figs. 12A, 12B, 16, 18, 19 and the accompanying descriptions. Other figures and description provide additional description and structure. There is nothing in claims 2, 6-8, 16 and 64 of copending Application No. 09/902,541 that teach such structure. Applicant maintains that there is nothing in claims 2, 6-8, 16 and 64 of copending Application No. 09/902,541 that even teaches the functions (detecting whether transitions of an input data stream fall into a predetermined portion of a clock period of a clock utilized to sample the input data stream or evaluating whether a phase-locked loop (PLL) has recovered a timing associated with the input data stream according to occurrence of transitions in the predetermined portion of the clock) recited in claim 16. Accordingly, applicant respectfully request that the rejection of claims 16 and all rejected claims dependent thereon be reconsidered and withdrawn.

In view of the above remarks, applicant believes that all claims are in condition for allowance and early notification to that effect is respectfully requested. If there are any issues which the Examiner believes could be resolved via a telephone interview, the Examiner is respectfully requested to contact the undersigned at the number indicated below.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

Mark Zagorin 11/21/02

Mark Zagorin Date

Respectfully submitted,

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